A HIGH SPEED AND LESS AREA MULTIPLIER FOR HIGH SPEED PROCESSOR BY SDT TECHNIQUE

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ABSTRACT

A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics. It generates all partial products and their sum in one step. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased. The modified Vedic multiplier is coded in Balsa Hardware Description Language which uses a syntax directed translation technique, synthesized and simulated using same EDA (Electronic Design Automation) tool.

KEYWORDS: Balsa, Carry Save Adder (CSA), Multiplication, Syntax Directed Translation (SDT), Urdhva Tiryagbhyam Sutra, Vedic Mathematics, and Vedic Multiplier (VM)